

Semiconductor BOM Wafer & Substrate Quality Checklist 2026

Wafer Material Specification Verification

Reviewing substrate purity levels, crystal orientation, and silicon/compound semiconductor thickness requirements against the BOM master record.

Wafer Material Type

Target Wafer Diameter (mm)

Crystal Orientation

☐ <100>☐ <110>☐ <111>

Impurity Concentration Limit (ppm)

Material Certificate of Analysis (CoA)

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Required Thickness Tolerances

- ☐ Standard Tolerance
- ☐ Ultra-Thin Specification
- ☐ High-Precision Spec

Verification Engineer Approval

Substrate Surface Integrity Inspection

Verification of surface roughness (Ra), flatness tolerances, and the absence of micro-defects or contaminants on the wafer surface.

Surface Roughness (Ra) Status

- ☐ Within Specification
- ☐ Out of Specification
- ☐ Requires Re-inspection

Measured Surface Roughness (Ra) Value

Enter a number...

Detected Surface Defects

- ☐ Scratches
- ☐ Pitting
- ☐ Particulate Contamination
- ☐ Micro-cracks
- ☐ None Detected

Defect Detail & Observation Notes

Write something...

Microscopic Imaging/SEM Report

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Quality Inspector Authentication

Chemical & Dopant Composition Audit

Ensuring all dopants, photoresist materials, and etching chemicals match the approved BOM chemical composition standards.

Dopant Concentration Level

Write something...

Purity Percentage

Enter a number...

Chemical Grade Classification

- ☐ Electronic Grade (Ultra-High)
- ☐ Industrial Grade
- ☐ Reagent Grade

Chemical Batch Expiry Date

Enter date...

Certificate of Analysis (CoA)

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Detected Impurities

- ☐ Carbon
- ☐ Oxygen
- ☐ Metallic Trace Elements
- ☐ None/Within Tolerance

Quality Assurance Approval

Layer Thickness & Deposition Accuracy

Validation of thin-film deposition thickness (dielectrics, metallization) and structural integrity of deposited layers per technical specifications.

Dielectric Layer Thickness (nm)

Enter a number...

Metallization Layer Thickness (nm)

Enter a number...

Deposition Method

- ☐ Chemical Vapor Deposition (CVD)
- ☐ Physical Vapor Deposition (PVD)
- ☐ Atomic Layer Deposition (ALD)
- ☐ Sputtering

Deposition Variance Notes

Write something...

Thickness Metrology Report

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Quality Engineer Approval

Part Number & Batch Traceability

Confirming that every wafer lot and substrate batch is mapped to unique IDs, manufacturer certificates of analysis (CoA), and origin documentation.

Primary Part Number

Batch/Lot ID Number

Manufacturing Date

Expiration/Shelf-life Date

Substrate Material Type

- ☐ Silicon (Si)
- ☐ Silicon Carbide (SiC)
- ☐ Gallium Nitride (GaN)
- ☐ Germanium (Ge)

Certificate of Analysis (CoA) Upload

 **Upload File**

Quality Assurance Inspector Sign-off

Contamination Control & Cleanroom Compliance

Audit of packaging materials and handling protocols to prevent particulate contamination and ensure ISO cleanroom compatibility.

Cleanroom ISO Class Verification

- ☐ ISO Class 1
- ☐ ISO Class 3
- ☐ ISO Class 5
- ☐ ISO Class 7

Daily Contamination Control Checkpoints Completed

- ☐ Air Particle Counter Calibration
- ☐ Surface Decontamination Protocol
- ☐ Gown/PPE Integrity Check
- ☐ Equipment Sterilization Log

Particle Count Per Cubic Meter

Enter a number...

Cleanroom Environmental Monitoring Report

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Last Sterilization/Decontamination Date

Enter date...

Quality Assurance Inspector Signature

Supplier Quality & Compliance Documentation

Verification of supplier-provided testing reports, RoHS/REACH compliance, and updated 2026 regulatory certification status.

Certificate of Analysis (CoA) Expiry Date

Enter date...

Supplier Compliance Certificate

 Upload File

Regulatory Compliance Status

- ☐ Fully Compliant
- ☐ Pending Verification
- ☐ Non-Compliant / Action Required

Verified Compliance Standards

- ☐ RoHS Compliant
- ☐ REACH Compliant
- ☐ ISO 9001 Certified
- ☐ Conflict Minerals Free

Supplier Audit Reference Number

Write something...

Quality Assurance Approval

Post-Processing & Packaging Readiness

Reviewing the compatibility of substrate dimensions with downstream dicing, thinning, and final assembly BOM requirements.

Substrate Compatibility Status

- ☐ Compatible with Assembly Line
- ☐ Requires Modification
- ☐ Incompatible / Hold

Target Dicing Margin (microns)

Required Post-Processing Steps

- ☐ Wafer Thinning
- ☐ Backgrinding
- ☐ Lapping
- ☐ Singulation/Dicing
- ☐ Polymer Coating

Scheduled Packaging Start Date

Post-Processing Specification Sheet

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Quality Assurance Inspector Sign-off

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✔ Finish

🔧 Generate Sample Report